

Notice of References Cited	Application/Control No. 10/760,998		Applicant(s)/Patent Under Reexamination LIU, FANG-BIN	
	Examiner Cynthia Britt		Art Unit 2117	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,891,395 B2	05-2005	Wells et al.	326/38
*	B	US-6,983,405 B1	01-2006	Herron et al.	714/726
*	C	US-6,996,758 B1	02-2006	Herron et al.	714/726
*	D	US-6,874,107 B2	03-2005	Lesea, Austin H.	714/725
*	E	US-6,651,238 B1	11-2003	Wells et al.	716/16
*	F	US-6,817,006 B1	11-2004	Wells et al.	716/16
*	G	US-5,717,701 A	02-1998	Angelotti et al.	714/30
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 09283729 A	10-1997	Japan	AZUMA, MOTOO	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	TDB-ACC-NO:NN931119, DISCLOSURE TITLE: Boundary Walking Sequences for Circuit Board Interconnect Test PUBLICATION-DATA: IBM Technical Disclosure Bulletin, November 1993, US VOLUME NUMBER:36, ISSUE NUMBER: 11, PAGE NUMBER:19 - 22, PUBLICATION-DATE: November 1, 1993 (19931101)
	V	"Testing and Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures" by Harris et al. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Publication Date: Nov 2002 Volume: 21, Issue: 11 On page(s): 1337- 1343 ISSN: 0278-0070 INSPEC Accession Number: 7462957
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.